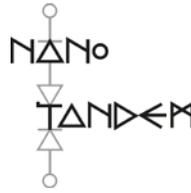


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Report on the electrical design of tandem cell

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Executive Summary

We here report on the electrical (combined with optical) modeling and theoretical design of a tandem solar of high (close to optimum) efficiency. The tandem cell consists of a top III-V nanowire cell and a bottom silicon cell. We have optimised a four-terminal device which is far simpler to fabricate than a two-terminal device and is in addition also predicted to have higher efficiency. Unintentional doping in intrinsic region is found to be a limiting factor of the top nanowire array cell efficiency. This unintentional doping may shift the junction position and change the p-i-n junction to a p-n junction. The unintentional doping in the intrinsic region should be two orders of magnitude lower than that of doping region. In top doping segment length, lack of sufficient electrical field limits the carrier splitting process which is detrimental for the efficiency. A nanowire top cell with 100 nm top doping segment leads to a 1 mA/cm² decreasing in short circuit current. Besides doping segment, the intrinsic segment is sensitive to surface quality. Long intrinsic region tends to increase the surface recombination and decreases solar cell efficiency.

The suggested four-contact electrical design parameters for the optimum nanowire array on silicon tandem cells are tabulated at the end of this report. The bottom silicon cell should be fabricated in the same way as in a recent publication from Fraunhofer.

Introduction and Motivation

The efficiency of nano-structured solar cell strongly depends on its geometry parameters and electrical properties. Carefully modeling is necessary to design a high-efficiency tandem solar cell. In a previous work by us, the geometry parameters of nanowire arrays on silicon tandem cells were studied with the aim of optimizing the absorption in the nanowire array [1]. An optical design of series connected double junction solar cell was determined with the best diameter, pitch and anti-reflection coating thickness. These optimized geometry parameters and thickness of anti-reflection coating can be used for both series connected (2-terminal) and independently connected (4-terminal) designs. As the 4-terminal design is predicted to have a higher efficiency [2], we have concentrated our efforts on this design, where we independently tune the top and bottom cell performance.

To optimise the electrical design, drift-diffusion equations are solved to determine the electrical properties of the nanowire array top cell. Three-dimensional solutions of these equations in nanowire array are computationally heavy and it is difficult to get converged results. In order to rectify this situation we developed one-dimensional modeling instead of three-dimensional modeling without sacrificing the accuracy of voltage-current response.

By applying this computationally fast one-dimensional model we studied solar cell performance of 2-micrometer long nanowire array top cell. Electrical parameters are listed with top cell parameters from modeling, and bottom cell fabrication details can be found in recent high-efficiency silicon cell [3].

Effect of Unintentional Doping in Intrinsic Region

In the modeling of the top nanowire array cell, 2-micrometer long GaInP/GaAsP nanowire p-i-n junction with an n-type doping on top of the nanowire is used as standard length. The bandgap of material is 1.7 eV. The thickness of doping segment is 100 nm for the top n-type doping and 1 micrometer for the intrinsic region if not specified. Note that all the conclusions are valid for longer wires with the change that one has to increase the bottom p-type segment length. GaInP is considered capped with SiO₂ or polymer directly and GaAsP is considered with a 10 nm III-V passivation shell and with SiO₂ as filling material. The effect of other contact and insulation layers can be found in [1].

Firstly, the doping levels of p-i-n junction are studied. The junction can split optically generated carriers efficiently when p (and n) type doping is at the level of 10^{17} - 10^{18} cm⁻³. The short circuit current does not depend on doping level in this doping region.

For the intrinsic region, unintentional doping usually goes in and changes the junction performance. In Figure 1, we studied the unintentional doping level in the intrinsic region. For both GaInP and GaAsP, when unintentional doping level approaches the level of p (or n) doped region, the p-i-n junction with a long depletion region tends to be p-n junction with a short depletion region. It results in a smaller carrier splitting efficiency and lowers down the short circuit current. As the optical generation in the nanowire mainly locates at a short region around the tip of the nanowire, n-type unintentional doping which shifts the junction position close to the middle of nanowire has a lower short circuit current, compared with p-type with the same unintentional doping level.

In brief, we suggest to control the doping level of the intrinsic region. It should be two orders of magnitude lower than top n segment doping level if it is n-type or one order of magnitude lower than bottom p segment doping level if it is p-type.

From this perspective, higher doping levels in p and n segments are good as the control of unintentional doping in i region is easier. On the other hand, the increasing of doping level in top n segment has a risk to increase Auger recombination [4]. We suggest an intentional p and n doping level of 10^{18} cm^{-3} as a balance between these two limitations.

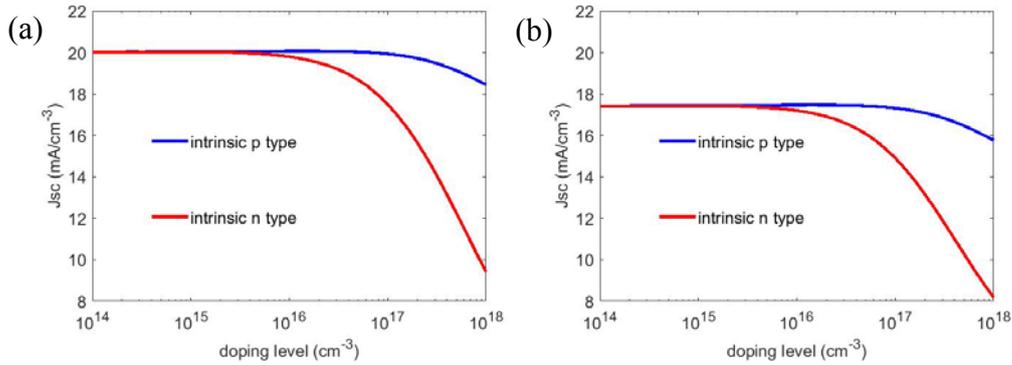


Figure 1: Short circuit current as a function of doping level in the intrinsic region of nanowire array top cell. p and n doping level: 10^{18} cm^{-3} . (a) GaInP nanowire array top cell length 2 micrometer. (b) GaAsP nanowire array top cell length 2 micrometer. The diameter, pitch and optical design of nanowire array are from [1] (structure 3).

Segment Length and Surface Passivation

In a p-n or p-i-n junction solar cell, top doping layer thickness is important for short circuit current. The lack of an electrical field in this layer leads to an insufficient optical carrier splitting process and result in a dead layer on top of the solar cell [5].

To reduce the electrical loss of this dead layer, the top doping layer should be small enough. In Figure 2, short circuit current as a function of top doping segment length is shown. A linear-like dependence of top segment length is observed. A top doping segment length of 100 nm can limit the decrease of short-circuit current within 5% (less than 1 mA/cm^2).

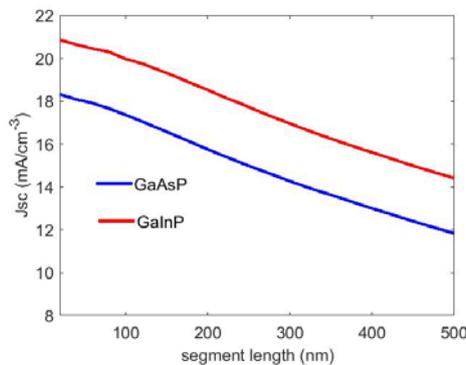


Figure 2: Short circuit current as a function of top n doping.

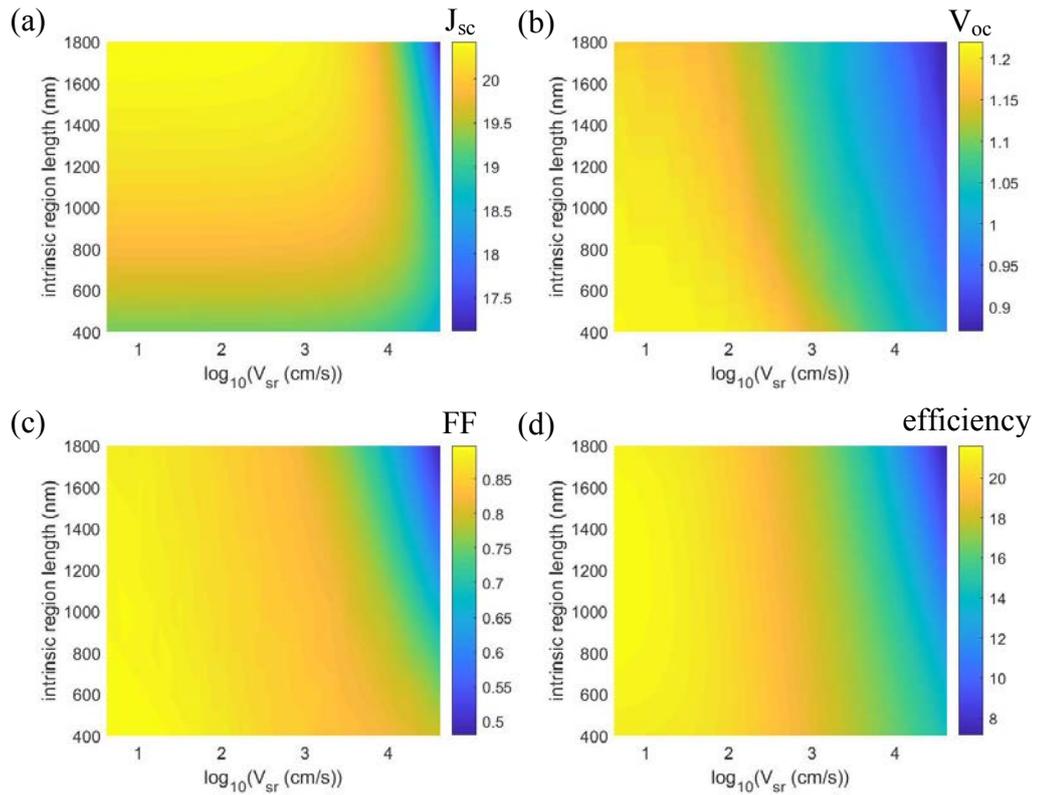


Figure 3: GaInP nanowire array solar cell performance as a function of intrinsic region length and surface recombination velocity. (a) Short circuit current (b) Open circuit voltage (c) Fill factor (d) Efficiency.

For the length of the intrinsic region, it depends on the balance of two limiting factors: the recombination in depletion region and the carrier splitting efficiency.

In Figure 3, the performance of GaInP nanowire is shown as an example to illustrate these two limiting factors. Firstly, a short intrinsic region of 400 nm is harmful to short circuit current due to the lack of electrical field. Thus lower splitting carrier efficiency lowers down the solar cell performance. Secondly, a longer intrinsic region increases the length of depletion region where the carrier has a larger probability to recombine. The open circuit voltage and fill factor drops down fast especially at high surface recombination velocity [6]. The similar effect holds true for GaAsP, see Figure 4.

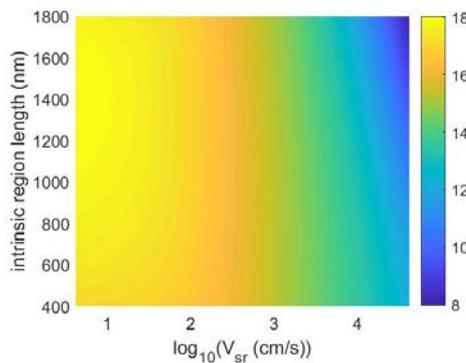


Figure 4: GaAsP solar cell efficiency as a function of surface recombination velocity and intrinsic region length.

We suggest the intrinsic region length to be in the range of 800-1000 nm. Assuming the surface passivation can suppress the surface recombination velocity to about 1000 cm/s, GaInP top cell with a length of 2 micrometers can reach the efficiency higher than 18%.

We summarized these electrical parameters in Table 1 together with silicon subcell electrical design [3].

Table 1: Electrical design for nanowire array top cell.

Top nanowire array cell (GaInP or GaAsP, bandgap 1.64eV -1.74 eV)	Diameter ⁺	170 nm (GaInP) 150nm with 10 nm passivation shell (GaAsP)
	Pitch ⁺	240 nm (GaInP) 210 nm (GaAsP)
	Length ⁺	2 μ m
	Top ITO contact layer ⁺	50 nm
	Top SiO ₂ anti-reflection layer ⁺	100 nm
	n-type doping	10^{18} cm ⁻³
	p-type doping	10^{18} cm ⁻³
	Intrinsic region	Unintentional doping < 10^{17} cm ⁻³ better to be 10^{16} cm ⁻³
	Top n doped segment length	100 nm* better to be smaller
	Intrinsic region length	800 nm to 1000 nm
	Bottom p doped segment length	The rest of nanowire*
	Surface recombination velocity	1000 cm/s
	Bottom silicon cell**	Emitter resistance p ⁺
Heavily-doped p ⁺⁺ emitter resistance		15 Ω /sq
Heavily-doped p ⁺⁺ emitter width		10 μ m
Front metal grid pitch		833 μ m
Front metal grid width		11 μ m

⁺ These parameters are from our recent publications [1].

*These suggested values are the same if p-type of nanowire is on top.

**Parameters are from [3] and similar fabrication can be done as in [3]. Contact and insulation layer design of top cell can be found in [1].

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